WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

a plurality of gate lines formed on an insulating substrate;

a gate insulating layer formed on the gate lines;

a semiconductor layer formed on the gate insulating layer;

a plurality of data lines formed at least in part on the semiconductor layer;

a plurality of drain electrodes formed at least in part on the semiconductor layer;

a plurality of pixel electrodes connected to the drain electrodes; and

a plurality of conductive lines, each conductive line connected to one of the gate lines and the data lines and including first and second portions having different resistances.

2. The thin film transistor array panel of claim 1, wherein each conductive line includes a lower film and an upper film having resistivity lower than the lower film and the first portion of each conductive line does not include the upper film.

3. The thin film transistor array panel of claim 2, further comprising a passivation layer disposed between the data lines and the pixel electrodes.

4. The thin film transistor array panel of claim 3, wherein the passivation layer has a plurality of first contact holes exposing the first portions of the conductive lines.

5. The thin film transistor array panel of claim 4, wherein the first contact holes expose edges of the first portions of the conductive lines.

6. The thin film transistor array panel of claim 4, wherein the passivation layer further has a plurality of second and third contact holes exposing portions of the gate lines and the data lines, respectively.

7. The thin film transistor array panel of claim 6, further comprising a plurality of contact assistants formed of the same layer as the pixel electrodes and connected to the gate lines and the data lines through the second and the third contact holes, respectively.

8. The thin film transistor array panel of claim 4, further comprising a plurality of protective members formed of the same layer as the pixel electrodes and covering the first portions of the conductive lines.

9. The thin film transistor array panel of claim 1, further comprising a plurality of ohmic contacts disposed between the semiconductor layer and the data lines.

10. The thin film transistor array panel of claim 1, w herein the semiconductor layer has substantially the same planar shape as the data lines and the drain electrodes except for portions located between the data lines and the drain electrodes.

11. The thin film transistor array panel of claim 1, further comprising a shorting bar connected to the conductive lines.

12. The thin film transistor array panel of claim 1, w herein the conductive lines extend to an edge of the thin film transistor array panel.

13. A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate line including an extension and a plurality of gate electrodes and a gate shorting bar on an insulating substrate, the gate line and the gate shorting bar including a first lower film and a first upper film having resistivity lower than the first lower film;

forming a gate insulating layer;

forming a semiconductor layer;

forming a data line including an extension and a plurality of source electrodes, a plurality of drain electrodes, and a data shorting bar on an insulating substrate, the data line, the drain electrodes, and the gate shorting bar including a second lower film and a second upper film having resistivity lower than the second lower film;

removing a first portion of the first upper film of the extension of the gate line and a second portion of the second upper film of the extension of the data line; and

forming a plurality of pixel electrodes connected to the drain electrodes.

14. The method of claim 13, wherein the first and the second lower films comprise Cr, Mo or Mo alloy and the first and the second upper films comprise Al or Al alloy.

15. The method of claim 14, further comprising:

forming a passivation layer between the drain electrodes and the pixel electrodes.

16. The method of claim 15, wherein the formation of the passivation layer comprises:

depositing the passivation layer; and

forming a plurality of contact holes exposing the first portion of the first upper film and the second portion of the second upper film.

17. The method of claim 16, wherein the removal of the first and the second portions is performed by blanket etching with an Al etchant.